CEL California Eastern Laboratories

Evaluation Board Document

µPC8233TK-EVAL-A

Evaluation Board

- Circuit Description
- Typical performance data
- Power gain and isolation plots
- Input and output return loss plots
- Circuit schematic and assembly drawing

Circuit Description

The circuit schematic and assembly drawing are shown on the last two pages.

Matching Circuits

The output matching is mainly through L3 and it should be placed close to the device.

The input matching consists of L1 and C2, and C1 is used for DC block For applications where noise figure is critically important, a high Q inductor, such as wire-wound type, is recommended over regular chip inductor for L1. Using high Q inductors can improve the noise figure by about 0.05dB. The values of L1 and C2 used on this evaluation circuit are chosen for a reasonable balance between input return loss and noise figure. A further trade-off can be made between these two parameters by adjusting the values of L1 and/or C2.

Desensitization Specifications

The desensitization data are shown in the next section for several frequency bands. This performance spec is strongly affected by the circuit topology of the input matching network as well as component values for given a topology. The matching circuit on this circuit is chosen for its relative simplicity and optimal balance between noise figure and input return loss. If any improvement on the desensitization spec is desirable at either higher or lower frequencies, a different set of component values or a different circuit topology may be used.

PCB Material

The PCB is FR4 four layer board. The top and bottom dielectric layers are 8mil thick. The total board thickness is 62mil.

Typical Performance Data

Test Conditions:

f=1575MHz; Vcc=Vps=2.7V

Noise Figure: 0.9dB (direct measurement on board, no subtraction of board loss)

Gain: 20dB

Input return loss: -12dB

Output return loss: -15.5dB

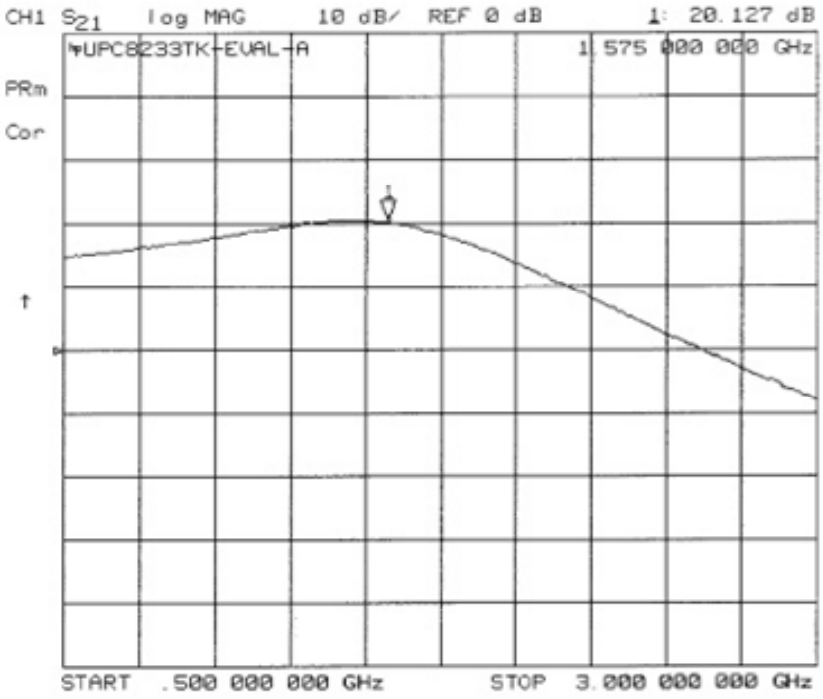
IP1dB: -21dBm

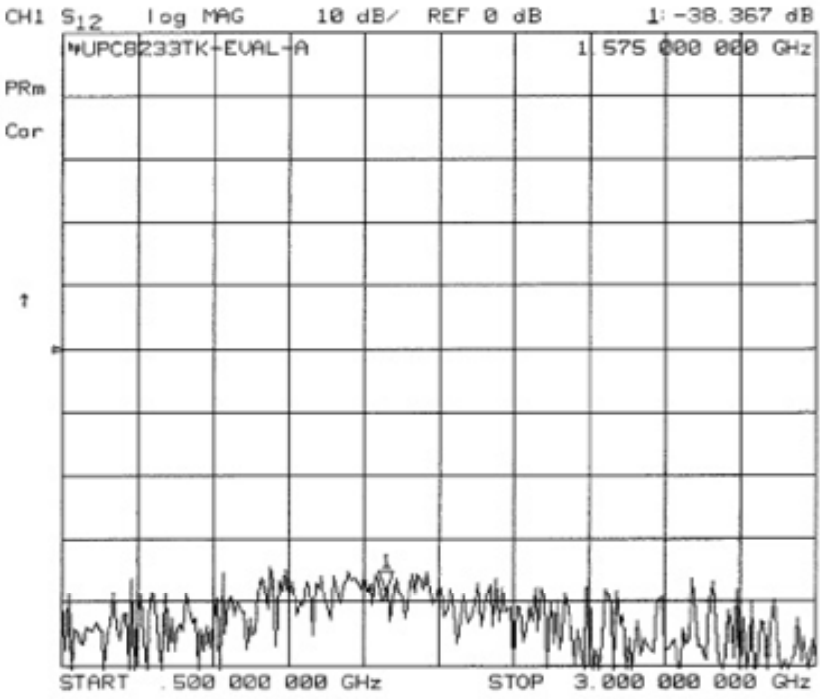
IIP3: -13dBm

P1dB desensitization due to out-of-band interfering signals: (The P1dB desensitization point is the power level of the interfering signal that causes a 1dB decrease in gain at 1575MHz.)

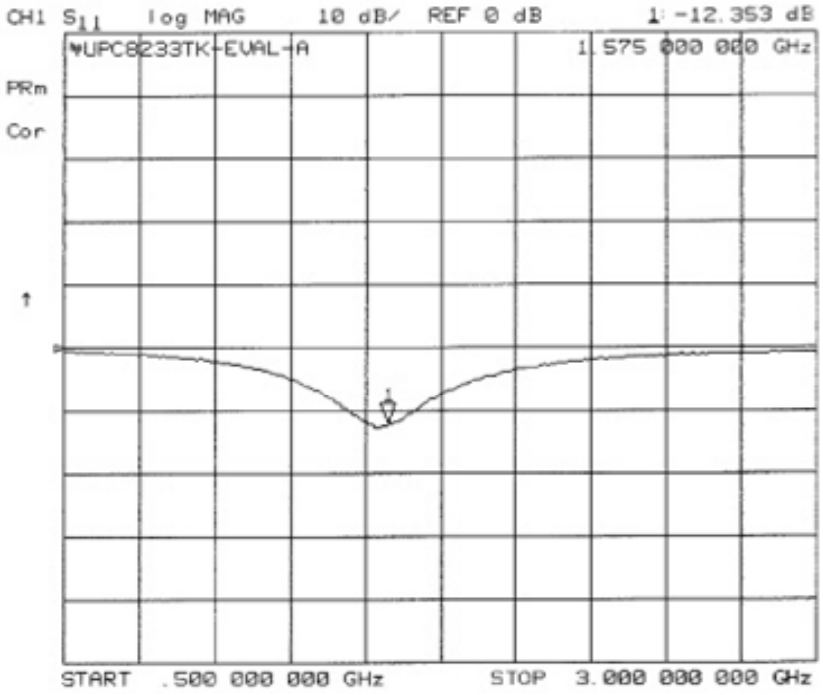
900MHz: -18dBm
1710MHz: -17dBm
1850MHz: -15dBm
2400MHz: -11dBm

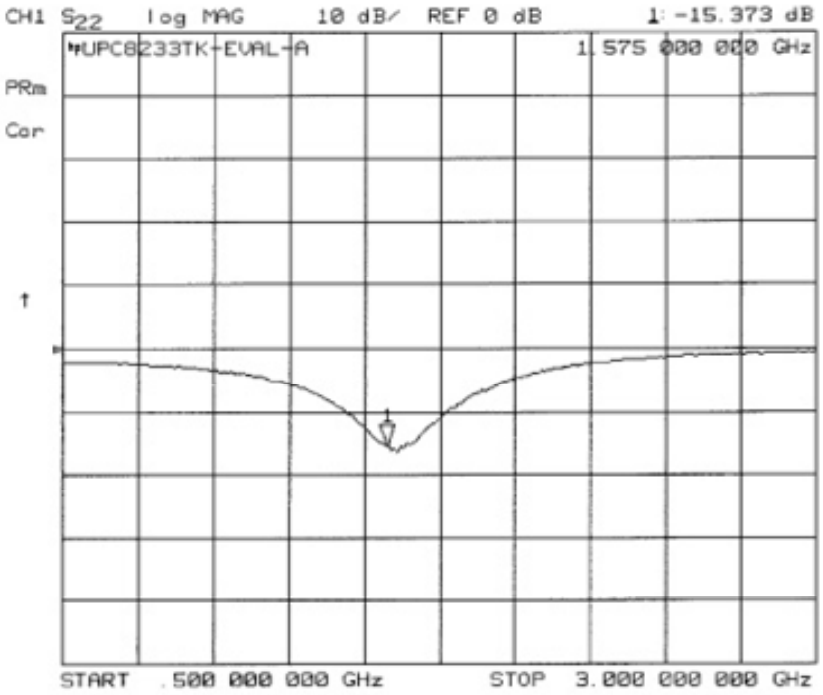
Power Gain and Isolation Plots



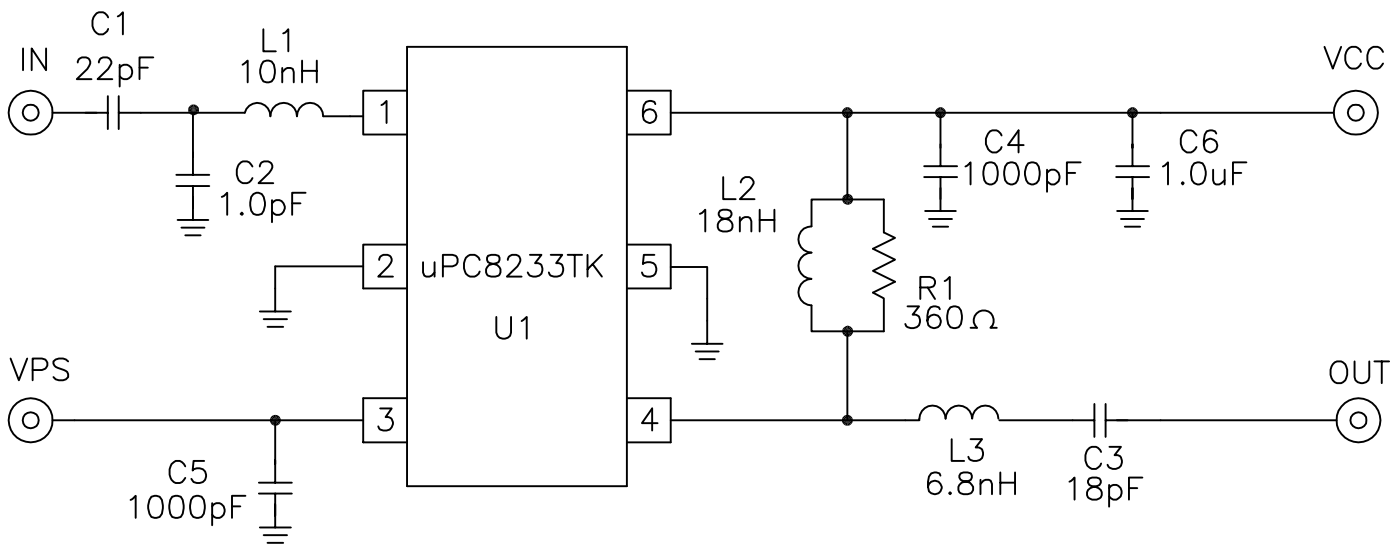


Input and Output Return Loss Plots





REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY	PART NUMBER OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.
1	LQG15HS6N8J02	L3	0402 6.8nH IND MURATA	14
1	LQG15HS18NJ02	L2	0402 18nH IND MURATA	13
1	LQW15AN10NG00	L1	0402 10nH IND MURATA WIREWOUND	12
1	RK73B1ETTP361J	R1	0402 360 OHMS RES KOA	11
1	GRM155R60J105KE19D	C6	0402 1.0uF CAP MURATA	10
2	GRM1555C1H102JA01D	C4,C5	0402 1000pF CAP MURATA	9
1	GRM1555C1H180JZ01D	C3	0402 18pF CAP MURATA	8
1	GRM1555C1H1R0CZ01D	C2	0402 1.0pF CAP MURATA	7
2	GRM1555C1H220J01D	C1	0402 22pF CAP MURATA	6
1	UPC8233TK	U1	IC NEC	5
3	2340-6111 TG	P1,P2,P3	PIN HEADER 3M	4
2	142-0711-821	J1,J2	SMA FEM. E.F. JOHNSON	3
1	CL-101738	DRAWING	COMPONENT LAYOUT DRAWING	2
1	N/A	PCB	PCB MANUFACTURED BY PCB NETWORKS	1

PARTS LIST

APPROVALS		
Drawing by:	BMU	06/06/2007
Designed by:	BMU	06/06/2007
Checked by:		
Project Engineer:		
Quality Control:		

CEL CALIFORNIA EASTERN LABS
4590 PATRICK HENRY DR. SANTA CLARA CA. 95054

TITLE:
UPC8233TK-EVAL-A
SCHEMATIC_BOM

SIZE	FSCM NO.	DWG NO.	REV
C		AD-101938	

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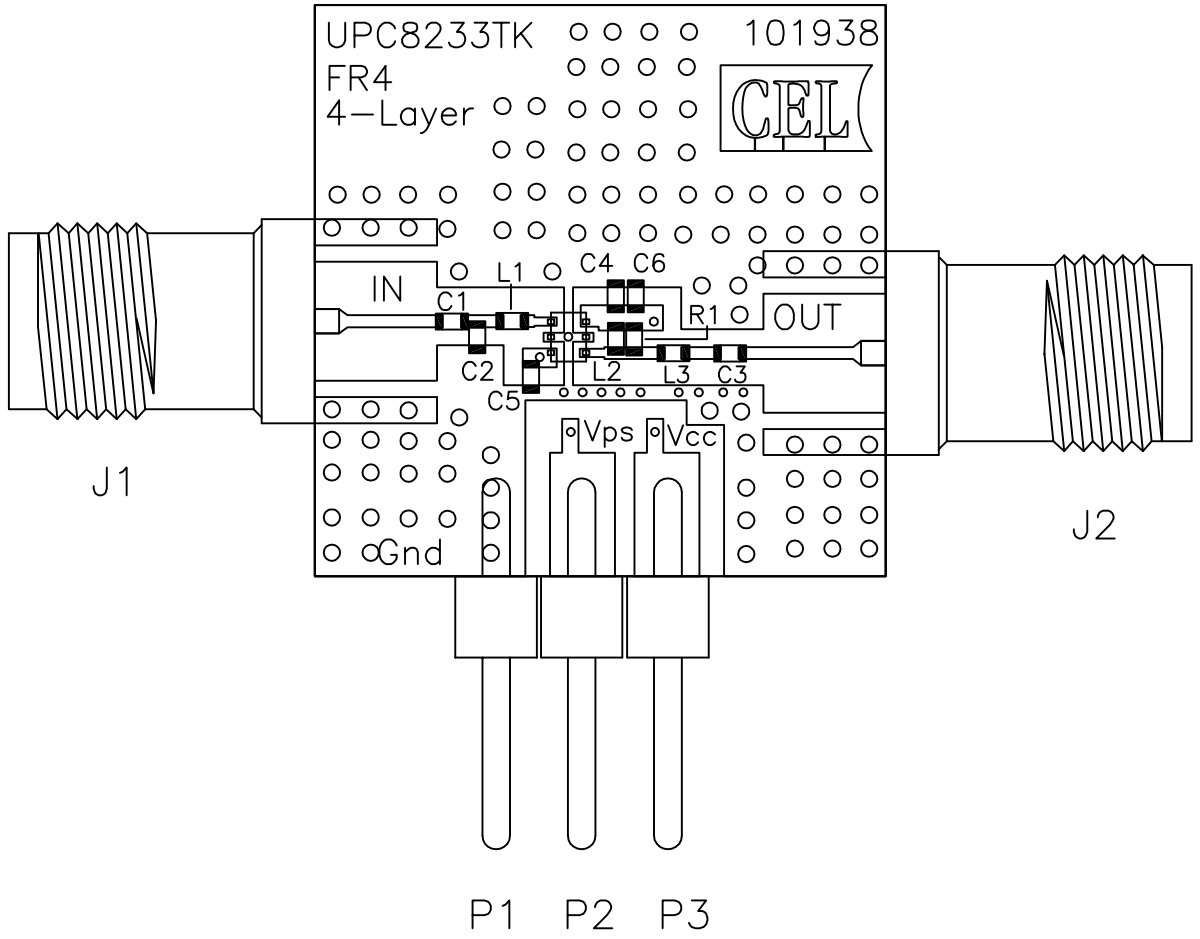
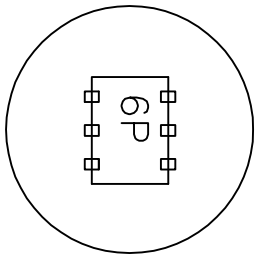
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED





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TITLE:
UPC8233TK-EVAL-A
ASSEMBLY_DRAWING

SIZE	FSCM NO.	DWG NO.	REV
C		AD-101938	-

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